REMARKS

Claims 1-8 and 12-23 remain pending in the application.

Claims 1-6, 17-19 and 22 over Persaud in view of Luan

Claims 1-6, 17-19 and 22 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Persaud et al., UK Patent Application No. GB2074762 ("Persaud") in view of Luan, U.S. Patent No. 5,911,149 ("Luan"). The Applicants respectfully traverse the rejection.

Claims 1-6 recite a second agent, receiving a first agent clock signal from a first agent, and providing a second agent clock signal to access a second portion of a non-dedicated **synchronous** memory including a second number of a plurality of memory banks. Claims 17-19 and 22 recite accessing external non-dedicated shared **synchronous** memory from a second agent based on a representation of a memory access clock signal that is in synchronism and in-phase with a memory access clock signal.

Persaud discloses an out-dated and rudimentary technique for synchronizing agents each accessing their own dedicated asynchronous dynamic random access memory (DRAM). A master one of the agents is given special access to interrupt operations by a slave agent and interject a memory access to the DRAM dedicated to that slave.

Simply put, Persaud fails to disclose synchronous memory, much less the use of synchronized clock signals between a plurality of agents accessing the same synchronous memory, as claimed by claims 1-6, 17-19 and 22.

Moreover, according to Persaud, the master generates synchronizing signals applied over a backplane to each of the slave agents. (Persaud, page 1, lines 45-46). Synchronization signals applied over a backplane are NOT clock signals, a **term of art**, routed between agents and for access of a synchronous memory, as recited by claims 1-6, 17-19 and 22.

Disadvantages of asynchronous DRAM are discussed at length in the background section of the current application. In particular, as explained in the text of the present application, increasing demands of high-end processors

have obsoleted asynchronous DRAM. (See, e.g., specification, page 2, lines 7-10)

Synchronous memory circuit designs are based on state machine operation instead of level/pulse width driven as in conventional asynchronous memory devices (Id at lines 10-12).

The bottom line is that Persaud utilizes very old late 1970s technology based on the use of level/pulse driven (e.g., R/W) signals. There is little similarity to today's synchronous memory systems. Moreover, one of ordinary skill in the art designing a computer system today would not have looked to art generated in the late 1970s for improvements.

The Office Action correctly acknowledged that Persaud additionally fails to disclose a first and second number of a plurality of memory banks being variable and a register to set at least one of the first and second number with a value set to correspond to a first number of the plurality of memory banks and a second number which is a remainder of the plurality of memory banks after the first number of the plurality of memory banks, which is adapted to be set by either one of agents (Office Action, page 3 and 4). However, the Office Action relies on Luan to allegedly make up for the deficiencies in Persaud to arrive at the claimed invention.

Luan discloses a computer system utilizing a shared memory used by a processor and any peripherals in the system (Abstract). The shared memory is a dynamic random access memory (DRAM) (Luan, col. 3, lines 46-48). The DRAM can include SDRAM that is configured by registers (Luan, Table 5).

Luan fails to even address the routing of clock signals to any of the components within the system, much less between the agents. Luan fails to disclose or suggest a second agent, receiving a first agent clock signal from a first agent, providing a second agent clock signal to access a portion of a non-dedicated synchronous memory, and accessing an external non-dedicated shared synchronous memory from a second agent based on a representation of a memory access clock signal that is in synchronism and in-phase with a memory access clock signal, as recited by claims 1-6, 17-19 and 22.

Moreover, application of synchronous memory to Persaud would most likely require a substantial redesign of the disclosed system to incorporate clock signal lines for synchronization. Such a substantial redesign is not suggested by Persaud's system designed for its intended purpose, much less Luan's use of SDRAM in an entirely different configuration.

Neither Persuad nor Luan, either alone or in combination, disclose, teach or suggest a second agent, receiving a first agent clock signal from a first agent, providing a second agent clock signal to access a portion of a non-dedicated synchronous memory, and accessing an external non-dedicated shared synchronous memory from a second agent based on a representation of a memory access clock signal that is in synchronism and in-phase with a memory access clock signal, as recited by claims 1-6, 17-19 and 22.

Accordingly, for at least all the above reasons, claims 1-6, 17-19 and 22 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 7,8, 12, 20, 21 and 23 over Wu in view of Persaud and Persaud in view of Wu

Claims 7, 8 and 12 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Wu et al., U.S. Patent No. 5,659,715 ("Wu") in view of Persaud, claims 20 and 21 rejected under 35 U.S.C. §103(a) as allegedly being obvious over Persaud in view of Wu, and claim 23 was rejected under 35 U.S.C. §103(a) as allegedly being obvious over Wu. The Applicants respectfully traverse the rejection.

Claims 7, 8 and 12 recite a plurality of agents, each receiving a common base clock signal from another agent and accessing an external non-dedicated shared synchronous memory with a memory access signal synchronized and in phase with the common base clock signal. Claims 20 and 21 recite a second agent that receives a clock signal from a first agent and generates a second agent clock signal for the second agent's access to a non-dedicated shared synchronous memory. Claim 23 recites accessing a second

plurality of synchronous memory banks from a second agent that receives a clock signal from a first agent.

Wu appears to disclose a first and second processor having access to a common memory bank (Fig. 3, items 302, 400 and 304 respectively). Address and data lines (Wu, items 306 and 308) running to the common memory bank (Wu, item 304) are routed through a single source, the graphics controller (Wu, item 400). The CPU (item 302) and the graphics controller are tied together to route data to the common memory (Wu, Fig. 3). The common memory is connected to the graphics controller which is connected to the CPU (WU, Fig. 3). A clock synthesizer interface provides for programming of a programmable clock synthesizer (Wu, col. 8, lines 39-43).

Wu discloses a system in which a CPU and a graphics controller utilize a common clock signal produced by a programmable clock synthesizer to access a common synchronous memory. Although Wu discloses two agents accessing a common synchronous memory, Wu does NOT disclose or suggest an agent receiving a clock signal from another agent, much less disclose or suggest an agent receiving a clock signal from another agent for access to a synchronous memory, as recited by claims 7, 8, 12, 20, 21 and 23.

As discussed above, Persaud fails to disclose or suggest an agent accessing synchronous memory, much less an agent receiving a clock signal from another agent for access to a synchronous memory, as recited by claims 7, 8, 12, 20, 21 and 23.

Neither Wu nor Persaud, either alone or in combination, disclose, teach or suggest an agent receiving a clock signal from another agent for access to a synchronous memory, as recited by claims 7, 8, 12, 20, 21 and 23.

At best, even if the combination of Wu and Persaud were obvious, which it is not, the theoretical combination would result in a system and method of using a CPU and graphics controller for accessing a common memory. A programmable clock synthesizer would provide a clock signal to the CPU, graphics controller and memory within the system. The CPU would send synchronization signals to the graphics controller. Even the theoretical combination fails to disclose or suggest an agent receiving a clock signal from

another agent, much less for access to a synchronous memory, as recited by claims 7, 8, 12, 20, 21 and 23.

Accordingly, for at least all the above reasons, claims 7, 8, 12, 20, 21 and 23 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 13-16 over Persaud in view of Muthal

Claims 13-16 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Persaud in view of Muthal, U.S. Patent No. 5,815,167 ("Muthal"). The Applicants respectfully traverse the rejection.

Claims 13-16 recite a second agent, receiving a first agent memory access clock signal from a first agent, and providing a second agent memory access clock signal to access a shared external non-dedicated **synchronous** memory.

As discussed above, Persaud fails to disclose synchronous memory, much less passing a memory access clock signal between a plurality of agents accessing the same synchronous memory, as claimed by claims 13-16.

The Office Action correctly acknowledged that Persaud additionally fails to disclose a first agent and a second agent accessing different portions of a shared external non-dedicted memory simultaneously (Office Action, page 10). However, the Office Action relies on Muthal to allegedly make up for the deficiencies in Persaud to arrive at the claimed invention.

Muthal appears to disclose a computer system comprising a graphics controller, a memory controller and shared memory (Abstract). The shared memory is accessible by both the memory controller and graphics controller (Muthal, Abstract). Concurrent access to portions of the shared memory is given to the graphics controller and the memory controller (Muthal, Abstract).

Although Muthal discloses a first and second agent accessing different portions of a shared non-dedicted memory memory simultaneously, Muthal fails to disclose how access to the shared portion of the memory system

is synchronized between the processor and the graphics controller. Muthal makes **no mention** of how clock signals are routed throughout the system.

Muthal fails to make up for the deficiencies in Persaud, i.e., fails to disclose or suggest a second agent, receiving a first agent memory access clock signal from a first agent, and providing a second agent memory access clock signal to access a shared external non-dedicated **synchronous** memory, as recited by claims 13-16.

Neither Persaud nor Muthal, either alone or in combination, disclose, teach or suggest a second agent, receiving a first agent memory access clock signal from a first agent, and providing a second agent memory access clock signal to access a shared external non-dedicated **synchronous** memory, as recited by claims 13-16.

Accordingly, for at least all the above reasons, claims 13-16 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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